High temperature smart-cut SOI pressure sensor

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ABSTRACT

Piezoresistive pressure sensors based on SMART CUT® SOI wafer have been developed, which can be used in extreme high temperature environments. It has been demonstrated that the resistance value of a heavily doped thin film (∼0.34 μm) resistor increases monotonically with temperature up to 600 °C. This is much higher than the maximum temperature of 330 °C normally shown in bulk silicon resistors. An analytical model is developed to explain how to extend the maximum operating temperature range based on doping effects and minority-carrier exclusion effects. Two types of packaging have been developed for different applications; one is for low pressure, high accuracy application, the other is for high pressure, high temperature application. The former is fully characterized across the range of 0.5–25 psi and –55 to 300 °C and the latter is calibrated across the range of 16–600 psi and –55 to 500 °C. A digitized curve fitting technique is used to calibrate the sensors by use of on-chip temperature signals. After curve fitting, the accuracy is <0.05% F.S. for the first type of the pressure sensor and <0.25% F.S. for the second type of the pressure sensor. A very low pressure hysteresis (<0.1% FS) at 500 °C indicates that the single crystal silicon diaphragm is capable of operating at very high temperature without creep or plastic deformation.

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1. Introduction

There is a growing demand for high temperature pressure transducers for use in extreme temperature environments such as aircraft gas turbine combustion control and chemical processing. Recently, many efforts have been focused on the design of a robust piezoresistive sensor for harsh environment applications based on wideband-gap semiconductors such as SiC, diamond, and GaN [1–5]. However, micro-fabrication technology of wideband-gap sensor materials is far less mature than silicon micromachining technology. There is still some distance to go for these wideband-gap sensors to become cost-effective products. Therefore, development of high temperature low-cost micromachined silicon piezoresistive transducers based on silicon-on-insulator (SOI) technology is still attractive [6]. A piezoresistive transducer is a DC driven component, unlike piezoelectric and capacitive transducers which require fragile controlled impedance wiring or expensive charge amplifiers. Furthermore, the whole structure of a piezoresistive sensor can be designed to sustain temperatures above 600 °C and the DC signal can be conveyed through a relatively long cable to a low cost electronic circuit which is located some distance away without significant degradation. One of the major factors affecting the performance of the piezoresistive pressure sensor is the temperature dependence of its pressure characteristics especially over a wide temperature range. The influence of temperature variation is manifested as a change in the span, bridge resistance, and offset of the sensor. Therefore, it is often necessary to compensate for temperature variations by measuring the temperature of the pressure sensor through a separate on-chip temperature sensor or by measuring current flow through the resistive bridge [7]. The temperature signals together with pressure output signal are then digitized through an analog-to-digital converter in a signal processing circuit. This circuit calculates a corrected pressure signal through a pre-programmed digital correction algorithm stored in a programmable read only memory [8]. This method is valid when the resistance value of silicon resistor monotonically increases with temperature until it reaches its critical temperature. At the critical temperature the silicon resistance value drops considerably making the calibration method ineffective. Therefore, the critical temperature is one of the key parameters for designing high temperature silicon piezoresistive pressure sensors.

However, the maximum operating temperature of a bulk silicon resistor is normally below 330 °C due to the excessive thermal generation of charge carriers at high temperature [8–11]. In order to extend the critical temperature of a silicon resistor, the silicon film on insulator (SOI) has been used to fabricate a high temperature sensor. It is found that the minority-carrier exclusion effect can reduce the number of thermally generated carriers and ultimately maintain extrinsic carrier concentration at the intrinsic temperature [12,13]. For example, by introducing a spreading-resistance structure using a 1.2 μm n-type low doping (1 × 10¹⁵ cm⁻³) SOI thin...
film, the maximum operating temperature can be increased up to 550 °C [14].

Polysilicon piezoresistive sensors have historically been classified as low performance devices due to its instability at high temperatures, especially at temperatures above 350 °C. Non-repeatability errors of polysilicon sensors are caused in part by grain growth and doping segregation in grain boundaries. Such errors are usually uncorrectable. Therefore, polysilicon films are unsuitable for high temperature pressure sensors.

In this work, ultra-thin single crystal films (less than 0.5 μm) of smart-cut® silicon-on-insulator are used as a sensing element to create high temperature piezoresistive pressure sensors. The completed pressure sensors are capable of operating up to 600 °C. An analytical model is developed to explain extension of operating temperature range in p-type SOI sensor.

2. Sensor design and fabrication

2.1. Chip design and wafer processing

Very thin active layer (0.34 μm thick) SOI wafers produced under the trademark SMART CUT® by Soitec are used as starting material. The buried oxide thickness is about 1 μm which enables the sensor to function at very high temperatures without any leakage effects associated with the p–n junction type devices. The silicon films are doped to the highest level (solid solubility) in order to achieve the most stable, long-term electrical performance characteristics of the sensing elements. P-type doping is selected for two reasons: First, the piezoresistive coefficient of single crystalline silicon is very much dependent on the crystal orientations and doping type. In order to obtain the highest sensitivity on a (1 0 0) silicon layer, p-type resistors can be easily arranged on the edge of a square diaphragm along with (1 1 0) direction as shown in Fig. 1, while n-type resistors have to be rotated 45° [15]. Therefore, the p-type resistor is favorable. Second, heavily doped p+-Si has less temperature dependence than heavily doped n+-Si.

After the film is doped with high dose boron ion implantation and anneal, four pressure sensing resistors are patterned with an RIE etch and joined together in a Wheatstone bridge configuration as shown in Fig. 1. A temperature-sensitive resistor is located on the device away from the diaphragm area. It has no response to diaphragm deflection when pressure is applied but it can sense the temperature change of the device. The temperature sensor allows the controller to use temperature-compensating techniques when analyzing the output of the sensing component. The passive layers SiO2/SiN are applied to the top of the resistors. Contacts are then photo patterned and etched using RIE. Proprietary high temperature metal ohmic contacts are formed to enable the device to be bonded with platinum wire so that the device is able to operate up to 600 °C. Micromachining is performed using the KOH etch process to create cavities on the backside of the wafer. In order to prevent the silicon diaphragm from being plastically deformed at high temperature and high pressure, the dimensions of the silicon diaphragm have been carefully chosen so that the maximum stress is well below the yield strength of 15,000 psi [16]. The wafer is then attached to a backing wafer with silicon pedestals by a fusion bond process. Finally, a capping wafer is attached to the device wafer by a high temperature glass frit to form a reference pressure chamber as shown in Fig. 2. The resistors are placed on the diaphragm such that two experience mechanical tension in parallel and the other two are perpendicular to the direction of current flow. Thus, the two pairs exhibit resistance changes opposite to each other. These pairs are located diagonally in the bridge such that applied pressure produces a bridge imbalance. According to piezoresistive theory, when the bridge is powered by constant voltage $V_B$, the voltage output due to mechanical deflection of the diaphragm is described by the following expression:

$$\Delta V = \frac{1}{2} \left( \frac{\Delta R_1}{R_1} - \frac{\Delta R_2}{R_2} \right) V_B$$  \hspace{1cm} (1)

Here assuming resistance variation ratio $\Delta R_1/R_1 = \Delta R_3/R_3$ and $\Delta R_2/R_2 = \Delta R_4/R_4$.

2.2. Packaging

Two package structures (HTSSPS-4008L and HTSSPS-4008H) are built as shown in Figs. 3 and 4. In Fig. 3, the sensor die is attached to a header plate through a silicon pedestal. The silicon pedestal acts as a thermal stress isolation member to reduce error generated by thermal mismatch between silicon and the header plate. However, the pressure applied to the diaphragm tends to pull the sensor die away from the header plate, so this package structure is usually used for low pressure measurements less than 200 psi. In contrast, in the second package design as shown in Fig. 4, the sensor die is mounted on the opposite side of the header plate relative to the structure of Fig. 3. The header plate is made of AlN which has a small thermal mismatch relative to the silicon pedestal. The pressure applied to the sensor die pushes the attachment joint in compression and thereby greatly increases the pressure capability of the pressure sensor and the die attach.

All electrical connections in both Figs. 3 and 4 are made by platinum wire bonding and can be protected in a vacuum or nitro-
3. Sensor characterization

Sensor calibration is a critical step to enable the piezoresistive pressure sensor to be accurate over a wide temperature range. The change in resistance due to temperature can be greater than the change in the pressure measurement. The resistors are arranged in a full bridge so that the change in temperature is a common mode effect acting on all resistors simultaneously, therefore, the temperature effects should cancel out. Due to manufacturing tolerances, the temperature coefficients of each resistor will invariably be slightly different. Therefore, temperature and pressure calibration is needed. During the calibration process the test system controller sets an oven at a desired temperature while a series of pressures are applied to the pressure sensor by a precision pressure source (Mensor PCS400). Data is taken at each applied pressure. Once all the data points for a particular pressure range have been obtained, the oven is changed to the next desired temperature and the above steps are repeated. After a series of temperature steps, polynomial coefficients are generated based upon curve fitting techniques. The coefficients are stored in a non-volatile memory for access and use by a microcomputer system. For example, the corrected pressure using a polynomial curve fitting of the fifth order of pressure and the fifth order of temperature is calculated as follows:

\[
P_{\text{corrected}} = C_0 + C_1 V_P + C_2 V_T + C_3 V_P^2 + C_4 V_P V_T + C_5 V_T^2 + C_6 V_P V_T^2 + C_7 V_P^2 V_T + C_8 V_P V_T^2 + C_9 V_P^2 + C_{10} V_P V_T + C_{11} V_T^3 + C_{12} V_P V_T^2 + C_{13} V_P V_T + C_{14} V_P V_T + C_{15} V_P^2 + C_{16} V_P V_T + C_{17} V_P^2 V_T + C_{18} V_P V_T + C_{19} V_P + C_{20} V_T^2
\]

where \(C_0, C_1, \ldots, C_{20}\) are the coefficients of polynomial, \(V_P\) and \(V_T\) are normalized pressure and temperature defined as follows:

\[
V_P = \frac{V_{\text{measured}, P}}{V_{\text{ref}}}
\]

\[
V_T = \frac{V_{\text{measured}, T}}{V_{\text{ref}}}
\]

The \(V_{\text{measured}, P}\) is the voltage output prior to correction and \(V_{\text{measured}, T}\) is the temperature signal from a voltage drop across an on-chip resistor \(R_T\). Alternatively one may use an off-chip sensing resistor that is electrically coupled to the bridge such that any change in the bridge current due to temperature change causes a change in voltage drop across the sense resistor. By using digital circuitry to process the above formula, the pressure measurement accuracy can be improved by an order of magnitude, from approximately 1–5% of full scale pressure error to 0.1–0.5% of full scale pressure error.

The temperature calibration is carried out in a high temperature oven. For the low pressure sensor (as shown in Fig. 3) being characterized across the range of 0.5–25 psi and −55 to 300 °C, the data can be taken at applied pressures of 0.5, 4, 8, 12, 16, 20, 25, 30, 16, 12, 8, 4, and 0.5 psi. The temperature profile is 50, 150, 200, 250, 300, 250,
200, 150, 50, 0, −55, 0, and 50 °C. A typical temperature cycle test result is shown in Fig. 6. The accuracy after curve fitting is 0.05% F.S. over the pressure range of 0.5–25 psi and temperature range of −55–300 °C. For the high temperature, high pressure sensor (as shown in Fig. 4) being characterized across the range of 16–600 psi and −55–500 °C, data can be taken at applied pressures of 16, 100, 200, 300, 400, 500, 600, 500, 400, 300, 200, 100, and 16 psi. The temperature profile can be 25, 200, 350, 500, 350, 200, 25 °C. A typical temperature cycle test result is shown in Fig. 7. The accuracy after curve fitting is 0.25% F.S. over the pressure range of 16–600 psi and temperature range of 55–500 °C. For the high temperature, high pressure sensor (as shown in Fig. 4) being characterized across the range of 16–600 psi and −55–500 °C, data can be taken at applied pressures of 16, 100, 200, 300, 400, 500, 600, 500, 400, 300, 200, 100, and 16 psi. The temperature profile can be 25, 200, 350, 500, 350, 200, 25 °C, −55, and 25 °C. A typical temperature cycle test result is shown in Fig. 7. The sensitivity is about 0.42 mV/psi at 25 °C and 0.29 mV/psi at 500 °C. The accuracy after curve fitting is better than 0.25% F.S. over the pressure range of 16–600 psi and temperature range of −55–500 °C. A very low pressure hysteresis (<0.1% F.S) indicates that the single crystal silicon diaphragm is capable of operating above 600 °C without significant creep or plastic deformation. Long term stability testing is carried out in a furnace by setting the temperature at 55–300 °C for a short period time.

4. Discussion

The maximum operating temperature (Tmax) is defined as intrinsic turn on temperature. At intrinsic temperatures the carrier concentrations in the silicon resistor increase dramatically due to thermal generation. As a result the resistance collapses with the positive temperature coefficient changing to negative. This collapse generally limits the temperature range of a silicon sensor. However, the temperature range can be extended significantly by the so called exclusion effect. The exclusion effect in a silicon resistor increases with bias current. Therefore Tmax of a silicon resistor can be higher by increasing current density.

The theoretical model of minority carrier exclusion can very well explain the extended temperature range in a SOI sensor. The modeling result matches very well to the sensor output over a wide temperature range [12,13]. However, those sensors are made of low-doping (1 × 1015 cm−3) n-type SOI, which is significantly different from the pressure sensor built in this work, made of heavily doped p-type SOI. Therefore, it is necessary to build an appropriate physical model to describe high temperature properties of p-type SOI. Suppose the thin film SOI resistor in Fig. 2 has width W, length L and x is the distance from metal contact. A current density J is applied to the sensor element. The model is developed as follows.

The well-known semiconductor transport equations based on the diffusion model are

\[ J_p = q\mu_p p E - kT \mu_p \nabla p \]  
\[ J_n = q\mu_n n E + kT \mu_n \nabla n \]

where E is the electric field, k is the Boltzmann constant, T is the operating temperature, \( J_p \) and \( J_n \) are the hole and electron current densities, and \( \mu_p \), and \( \mu_n \) are the hole and electron mobility, respectively. Assuming space-charge neutrality, we have \( p = N_A + n \) and \( J_n = J - J_p \) and mobility ratio \( b = \mu_n / \mu_p \). By neglecting the diffusion terms (\( \nabla n \) and \( \nabla p \)) and eliminating E from Eqs. (5) and (6), we find

\[ J_n = \frac{n_j}{n + b p} \]

Since the silicon film is very thin, the current in the y and z directions are assumed to be zero. In the case of carrier exclusion, \( G \) is the constant generation rate and ignoring recombination.

\[ \frac{dn}{dx} = qG \]

and

\[ G = \frac{1}{\tau} \frac{n_i^2}{N_A + 2n_i} \]

where \( n_i \) is the intrinsic carrier concentration; \( \tau \) is excess-carrier lifetime (it is taken to be 2 μs in p-type silicon); \( N_A \) is the doping level of p-type SOI film. Integrate both sides of Eq. (8) from 0 to x and combine with Eq. (7) by assuming injected minority current at \( x = 0 \) is zero, results in

\[ n(x) = \frac{qGbN_A x}{f - qG(1 + b^2)x} \]
The resistivity of the sensor in exclusion region is given by

\[ \rho(x) = \frac{1}{q\mu_n R(x) + q\mu_p P(x)} \]  

(11)

Inserting \( p(x) = n(x) + N_A \) (assuming space-charge neutrality) into Eq. (11) results in

\[ \rho(x) = \frac{J - qG(1 + b')x}{q\mu_p N_A} \]  

(12)

Using \( J = I/(Wt) \), \( t \) is the SOI film thickness; the resistance of the sensor can be calculated as

\[ R = \frac{1}{Wt} \left[ \int_0^L \rho(x)dx + \int_{x_0}^L \rho_0 dx \right] = \frac{x_0}{q\mu_p N_A Wt} - \frac{G(1 + b')x_0^2}{2\mu_p N_A L} + \frac{1}{Wt} \left( \frac{b'(L - x_0)}{q\mu_p b' N_A + q\mu_p (1 + b')p_0} \right) \]  

(13)

\[ x_0 = \left[ qGbN_A + qG(1 + b)\rho_0 \right] \]  

(14)

where \( x_0 \) is the length of the exclusion region, when \( x = x_0 \) the minority carrier concentration reaches its equilibrium value \( n_0 = n_i^2/p_0 \); under low doping and high current condition, \( x_0 \) can be larger than \( L \). But for high doping, low current condition, \( x_0 \) is normally less than \( L \). Therefore, we set \( x_{\text{exc}} = \min(x_0, L) \); \( p_0 \) is an equilibrium resistivity, \( n_0 \) and \( p_0 \) are equilibrium hole concentration; The material parameters are as follows [12,17–19],

\[ \mu_p = 49.7 + \frac{479.37}{1 + \left( \frac{T}{300} \right)^{-3.7}} \times \frac{1 + 10^{6}}{10^{17}} \]  

(14)

\[ \mu_n = 55.24 + \frac{1429.23}{1 + \left( \frac{T}{300} \right)^{-3.8}} \times \frac{n_i + p_0}{10^{12}} \]  

(15)

\[ n_i = 5.71 \times 10^{19} \left( \frac{T}{300} \right)^{2.365} e^{-6733/T} \]  

(16)

\[ E_g(T) = 1.17 - \frac{4.73 T^{-4}}{T + 636} \]  

(17)

\[ p_0 = \frac{1}{2} \sqrt{N_A^2 + 4n_i^2 + N_A} \]  

(18)

\[ n_0 = \frac{1}{2} \sqrt{N_A^2 + 4n_i^2 - N_A} \]  

(19)

In the case of low doping concentration \( (N_A = 1 \times 10^{15} \text{ cm}^{-3}) \), the minority-carrier exclusion effect is strong. The third term in Eq. (13) can be neglected if \( L \) is selected to be less than or equal to the length of exclusion region \( x_0 \). The maximum operating temperature is dependent on the current density. Thermally generated minority carriers are suppressed by current produced majority carriers. When the \( W, L \) and \( I \) are fixed, the thinner the film, the higher the current density, thus the higher \( T_{\text{max}} \). Fig. 9 shows the calculated temperature characteristics of 10 \( \mu \)m \times 10 \( \mu \)m resistor with 0.01 mA bias current for different film thicknesses. As it is seen in Fig. 9, the \( T_{\text{max}} \) increases from 280 °C to around 500 °C when film thickness changes from 10 \( \mu \)m to 0.1 \( \mu \)m.

In the case of high doping concentrations \( (N_A \geq 5 \times 10^{17} \text{ cm}^{-3}) \), the thermally generated carrier concentration is far less than the majority carrier concentration. The length of minority carrier is only a couple of microns (i.e. \( x_0 \ll L \)). The third term in Eq. (13) becomes a dominator factor. The increase of current density no longer induces a strong carrier exclusion effect. Therefore, doping concentration has significant impact on \( T_{\text{max}} \) for the films with relatively high doping level. The calculated temperature characteristic of 0.34 \( \mu \)m thick SOI resistors as a function of doping concentration is shown in Fig. 10. The dimensions of the resistor are \( W = 10 \mu \text{m} \) and \( L = 2700 \mu \text{m} \), the current is 0.01 mA. The \( T_{\text{max}} \) increases from 230 °C to around 580 °C when doping concentration changes from \( 1 \times 10^{15} \text{ cm}^{-3} \) to \( 1 \times 10^{18} \text{ cm}^{-3} \). The calculated result indicates that doping concentration does have great influence on \( T_{\text{max}} \). It explains why measured temperature dependence of the resistance of 0.34 \( \mu \)m heavily doped SOI resistor shows \( T_{\text{max}} = 600 \circ C \) as shown in Fig. 8.

However, the calculated \( T_{\text{max}} = 600 \circ C \) corresponds to a sheet resistance of 77 ohm/□ at room temperature. It corresponds a doping level of \( N_A = 2 \times 10^{18} \text{ cm}^{-3} \). While the measured \( T_{\text{max}} = 600 \circ C \) of the sensor resistor corresponds to a sheet resistance of 27 ohm/□ at room temperature, this corresponds to doping of \( 1 \times 10^{18} \text{ cm}^{-3} \). The deviation between the calculated value and measured data indicates that Eq. (13) is not accurate enough to describe temperature characteristics of SOI thin film resistors. A more accurate theoretical model has to be generated by taking into account the impurity-induced band-gap narrowing effect which happens in degenerate semiconductors.

5. Conclusion

In summary, we have demonstrated that the maximum operating temperature of a piezoresistive device based on smart-cut@SOI is able to increase monotonically with temperature up to 600 °C. The smart-cut@SOI together with high temperature metal ohmic contacts, platinum wire bonds and special die attach materials enable these pressure sensors to operate reliably in extreme environments. The completed pressure sensors of HTSSPS-4008L and HTSSPS-4008H exhibit very low hysteresis, excellent repeatability, and long...
term stability. An analytical model is developed to explain how to extend operating temperature range by minority-carrier exclusion effect and doping effect. There are two ways of increasing $T_{\text{max}}$. The first way is to increase current density. For a low doping SOI sensor, the $T_{\text{max}}$ can be raised by thinning the film thickness for a fixed current. The second way is to increase doping concentration in sensing films. For a heavily doped SOI sensor, the minority-carrier exclusion effect is no longer valid. Doping effect has significant impact on $T_{\text{max}}$. The higher the doping level, the higher the $T_{\text{max}}$.

References